

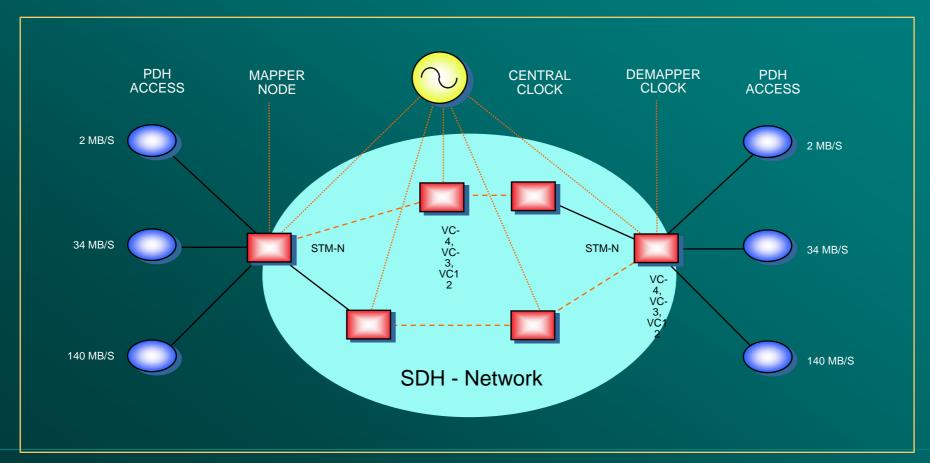
承包廠商:台灣國際標準電子股份有限公司日期:2005/5/23 - 2005/5/26



信號同步的重要性



The SDH network require synchronization due to its structure





信號同步的重要性



- Channels are byte-wise synchronously multiplexed
- A channel is identified by the phase of a specific byte relative to the frame as given by a pointer value.
- ◆ 輸入之同步信號由同步指標處理器進行同步。
- ◆ 若一個及多個SDH多工機未適當地同步化,SDH網路會產生同步 指標調整頻率及相位差異
- ◆ 最差狀況下,同步指標能指揮未配置同步之PDH信號中過度的 抖動jitter及漂移



信號同步的目的



- Generally the performances of a SDH network will be function of:
 - □ The quality of the synchronization signal supplied to the nodes.
 - ☐ The availability of this, i.e. the warranty of a defined quality level also in presence of failures in the distribution network.

 Availability requirement can be satisfied if the distribution network is able to support adequate protection schemes.



同步信號之階層



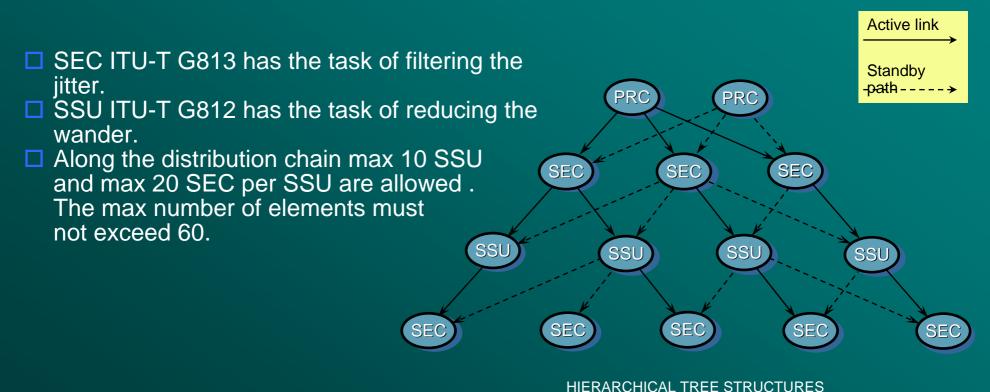
Levels of Synchronization				
PRC-LEVEL	PRC	Primary Reference clock	G.811 10E-11 Long term Frequency departure	
SSU-LEVEL	SSUL	Synchronization supply Unit/Transit node Synchronization supply Unit/Local node	5*10E-9 Accurancy G.812T 5*10E-10 Offset 10E-9/Day Drift 10E-7 Accurancy G.812L 10E-8 Offset 2*10E-8/Day Drift	
SEC-LEVEL	SEC	Synchronous Equipment clock	4.6*10E-6 Accurancy G.813 5*10E-8 Offset 5*10E-7/Day Drift	



同步網路架構(1)



◆ 主要應用為三階層樹支狀架構並搭配備援同步信號路由:

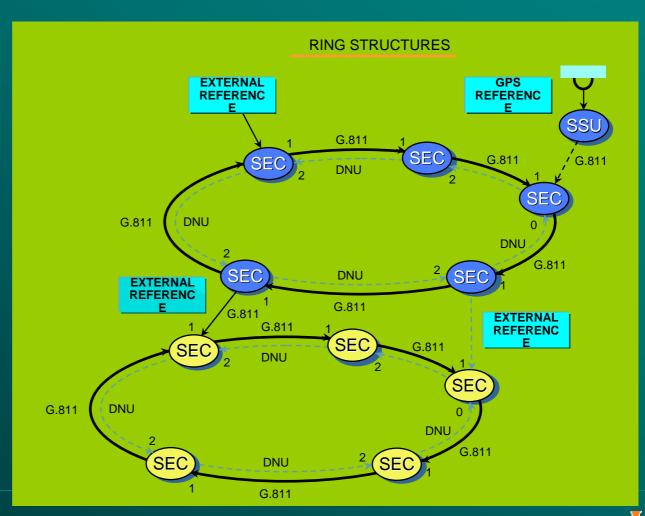


同步網路架構 (2)



byte (SSM)主要的 能為重置及回確保 步信號路由並確保 一步信號路由不會 造成迴路

- Synchronization input cannot be selected
- 1 Synchronization input has first priority
- 2 Synchronization input has second priority



同步網路架構(3)



◆ 同步狀態信息位元SSM為置放於STM-N信號之S1位元 或2 Mb/s 信號中之0時槽(time slot 0). 其數值代表6種不同的同步信號品質

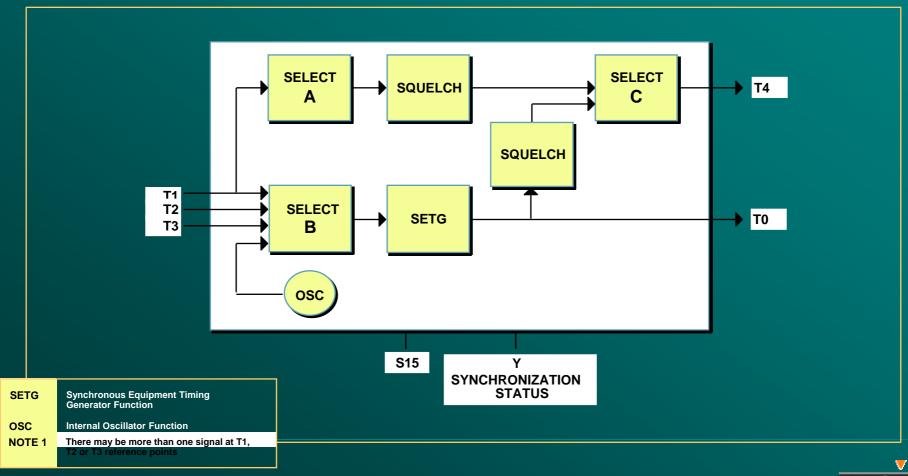
Synchronization Status Message Byte

QUALITY LEVEL	CODE	ORDER
QL-PRC	0010	HIGHEST
QL-SSU TRANSIT	0100	I
QL-SSU LOCAL	1000	I
QL-SEC	1011	I
QL-DNU (DO NOT USE)	1111	LOWEST
QUALITY UNKNOWN	0000	-



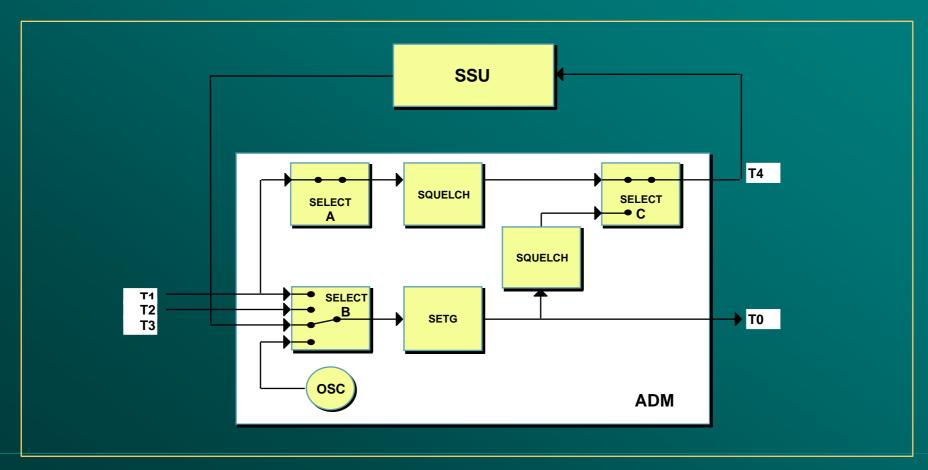
同步設備時脈 (SETS) 功能





ADM 多工機及SSU同步時鐘源運作關係







ADM 多工機及SSU同步時鐘源



- QL of incoming external reference T3 is drawn to:
 - □ QL of timing reference selected to generate T4
 - QL of SSU internal oscillator if T4 is squelched
- T4 is squelched when QL of timing reference is lower than SSU internal oscillator
- QL of SSU is defined/inserted via LCT/OS
- QL of T3 inputs can be forced/modified via LCT/OS.



ADM 多工機及SSU同步時鐘源



- QL of output timing references is set to:
 - □ QL of timing reference selected to generate T4 when SEC is locked to T3. QL6 is transmitted back to the source of T4.
 - □ QL of SSU when T4 is squelched
 - QL of SEC IO when no references are available
 - □ QL of a timing reference selected to generate T0 when T3 from SSU fails. QL6 is transmitted back to the source of T0.
- LCT/OS may provide for each output a QL which overule the previous ones.
- Link between T4 and SSU represents a weak point.



外部指令



- ♦ 鎖定Lock/解除Unlock
- ♦ 強制選取Forced selection
- ♦ 手動選擇 Manual Selection





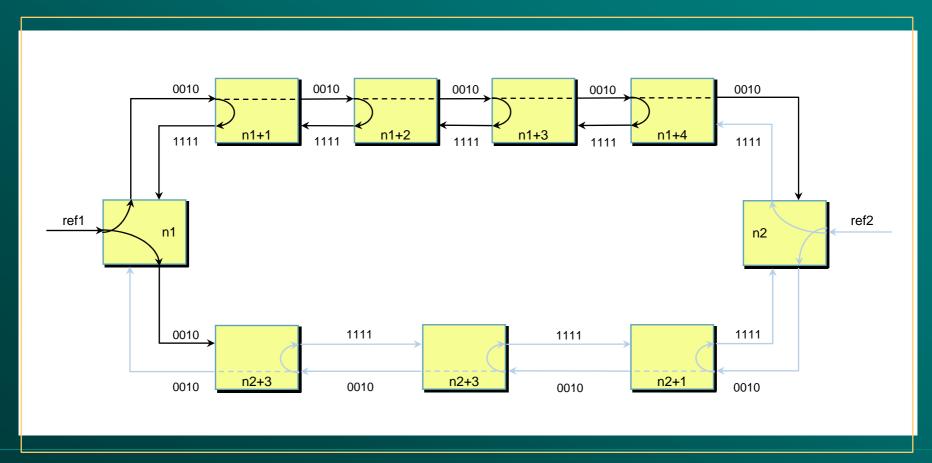
同步網路範例



同步網路範例(1)



Example 1: Ring with two external timing references in Normal Operation

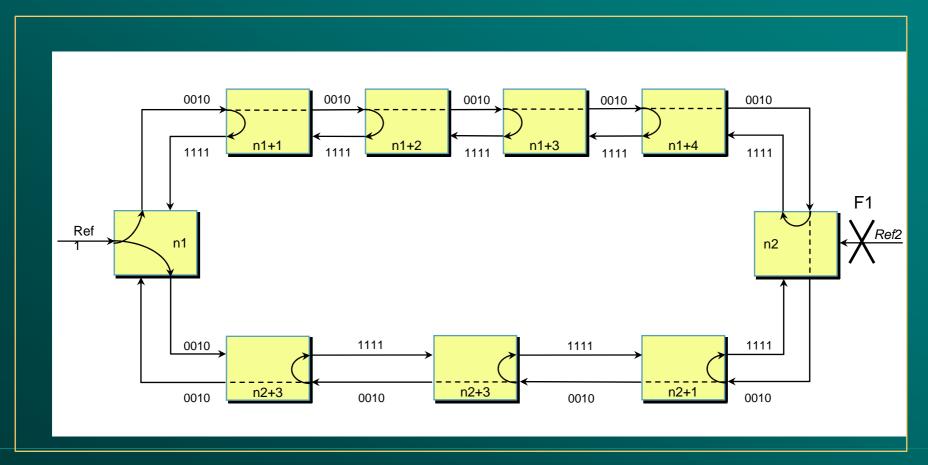




同步網路範例(2)



Example 1 : Reconfiguration caused by the loss of Ref2

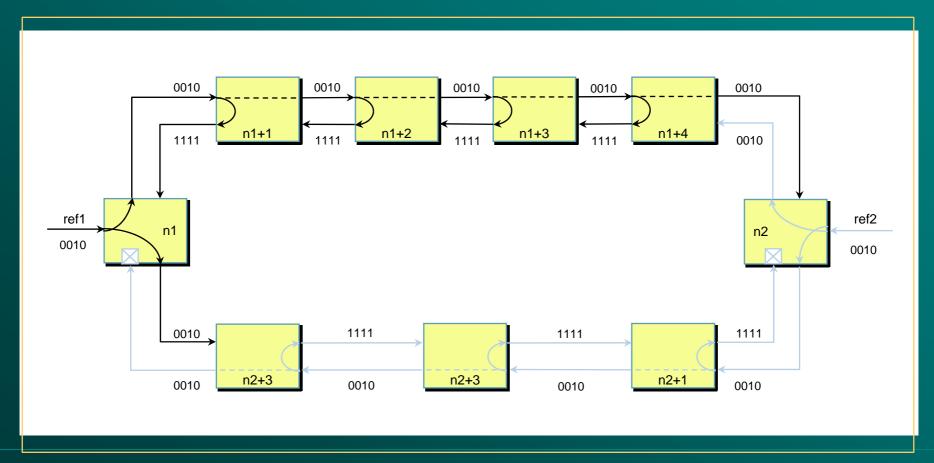




同步網路範例(3)



Example 2 : Ring with two external timing references in Normal Operation

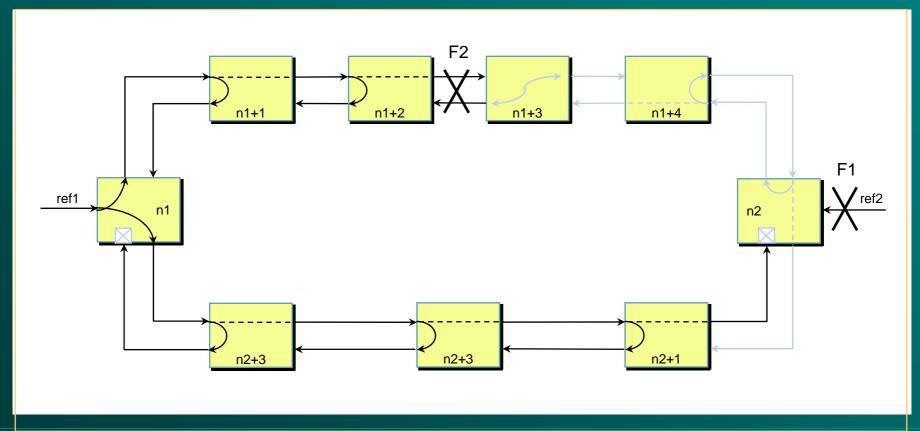




同步網路範例(4)



Example 2 : Reconfiguration caused by the loss of Ref2 and a link failure ---> two plesiochronous islands are produced





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簡報完畢恭請指導

